AMENDMENTS TO THE CLAIMS

This listing of claims replaces all prior versions and listings of claims in the application:

Listing of Claims

1. – 5. (Canceled)

6. (Currently Amended) ~~An electrical device according to claim 1,~~

An electrical device for efficient and flexible control of memory access, the device comprising:

at least two access channel circuits, wherein at least one of the access channel circuits is connected to at least one memory accessing unit via at least one system bus and to at least one physical memory module, of a memory, wherein the at least one physical memory module comprises a first physical memory module and a second physical memory module;

the at least one access channel circuit providing memory access for the at least one memory accessing unit to at least a part of the memory, wherein at least one of the access channel circuits further comprises an automatic data transfer engine for transferring data/information from the first physical memory module of the memory to the second physical memory module of the memory prior to the at least one memory accessing unit retrieving the data/information.

7. (Previously Presented) An electrical device according to claim 6, wherein each of the at least two access channel circuits comprises an automatic data transfer engine, the automatic data transfer engines being connected to form a chain of automatic data transfer engines where each data transfer engine is responsible for transferring a different part of the data/information.

8. (Currently Amended) ~~An electrical device according to claim 3,~~ An electrical device for efficient and flexible control of memory access, the device comprising:

at least two access channel circuits, wherein at least one of the access channel circuits is connected to at least one memory accessing unit via at least one system bus and to at least one physical memory module, of a memory;

the at least one access channel circuit providing memory access for the at least one memory accessing unit to at least a part of the memory;

a control and configure circuit configured to dynamically control the at least two access channel circuits, the control and configure circuit allowing for an addition of additional access channel circuits;

wherein at least one of the access channel circuits comprises at least one special purpose register and is connected to the control and configure circuit, wherein the control and configure circuit is adapted to modify a content of the at least one special purpose register thereby allowing for reconfiguration of at least one of the access channel circuits without affecting another one of the access channels during an operation of the device.

9. (Previously Presented) An electrical device according to claim 8, wherein the at least one special purpose register is adapted to reconfigure at least one of the access channel circuits by configuring a mode of functionality and/or at least one access region of the memory.

10. (Canceled).

11. (Currently Amended) ~~An electrical device according to claim 1,~~ An electrical device for efficient and flexible control of memory access, the device comprising:

at least two access channel circuits, wherein at least one of the access channel circuits is connected to at least one memory accessing unit via at least one system bus and to at least one physical memory module, of a memory, the at least one access

channel circuit providing memory access for the at least one memory accessing unit to at least a part of the memory;

wherein the at least one memory module comprises a plurality of memory modules and the at least one access channel circuit comprises:

a memory access controller adapted to monitor an incoming system bus, connected to one of the memory accessing units, and an outgoing system bus connected to the memory accessing unit for a first identifier representing a given memory bus to be connected, the memory access controller providing a first control signal/code, based on the first identifier, representing the given memory bus and to where the given memory bus is to be connected,

a source and destination selector for enabling access to a memory bus, connected to one of the memory modules of the memory, from the incoming system bus or the memory access controller dependent on the first control signal/code received from the memory access controller, and

a memory module selector for selecting which of the memory modules is to be connected to the outgoing system bus, connected to the memory accessing device, during a given read access of one of the memory modules dependent on a second unique identifier.

12. – 16. (Canceled)

17. (Previously Presented) ~~A method according to claim 12,~~ A method of control of memory access between at least one memory accessing unit and a memory comprising at least one physical memory module, the method comprising the steps of:

providing, with at least one of at least two access channel circuits, memory access for the at least one memory accessing unit to at least a part of the memory, wherein the at least one access channel circuit is connected to the least one memory accessing unit via at least one system bus and to the at least one physical memory module and wherein the at least one memory module comprises a first memory module and a second memory module~~, the method further comprising:~~ ; and

providing automatic data transfer of data/information with the access channel circuit, the access channel circuit comprising an automatic data transfer engine for transferring data/information from the first physical memory module of the memory to the second physical memory module of the memory prior to the memory accessing unit retrieving the data/information.

18. (Previously Presented) A method according to claim 17, wherein the automatic data transfer engine comprises a plurality of data transfer engines, and the access channel circuit comprises a plurality of access channel circuits, wherein

the plurality of automatic data transfer engines of the plurality of access channel circuits are connected to form a chain of automatic data transfer engines and

wherein each data transfer engine is responsible for transferring a portion of the data/information.

19. (Previously Presented) ~~A method according to claim 14, further comprising:~~ A method of control of memory access between at least one memory accessing unit and a memory comprising at least one physical memory module, the method comprising the steps of:

providing, with at least one of at least two access channel circuits, memory access for the at least one memory accessing unit to at least a part of the memory, wherein the at least one access channel circuit is connected to the least one memory accessing unit via at least one system bus and to the at least one physical memory module;

dynamically controlling the at least two access channel circuits with a control and configure circuit, the control and configure circuit allowing for an addition of additional access channel circuits; and

modifying, with the control and configure circuit, a content of at least one special-purpose register, wherein at least one access channel circuit of the at least two access channel circuits is connected to the control and configure circuit, thereby allowing for reconfiguration of the at least one access channel circuit without affecting another one

of the at least two access channel circuits during an operation of the access channel circuits.

20. (Previously Presented) A method according to claim 19, further comprising configuring a mode of functionality and/or at least one access region of the memory.

21. (Canceled)

22. (Currently Amended) ~~A method according to claim 22~~ A method of control of memory access between at least one memory accessing unit and a memory comprising at least one physical memory module, the method comprising the steps of:

providing, with at least one of at least two access channel circuits, memory access for the at least one memory accessing unit to at least a part of the memory, wherein the at least one access channel circuit is connected to the least one memory accessing unit via at least one system bus and to the at least one physical memory module, wherein the at least one memory accessing unit comprises at least two memory accessing units and the at least one memory module comprises a plurality of memory modules; and

providing memory access by one of the at least two access channel circuits for each connected one of the at least two memory accessing units where each of the at least two access channel circuits is connected with each of the plurality of memory modules of the memory; wherein the at least one memory accessing unit comprises a plurality of memory accessing units~~, the method further comprising:~~;

monitoring, with a memory access controller for a first identifier representing a given memory bus to be connected, the memory access controller comprising the access channel circuit, an incoming system bus, connected to one of the memory accessing units, and an outgoing system bus connected to another one of the memory accessing units;

providing, with the memory access controller, a first control signal/code, based on the first identifier representing the given memory bus and to where the given memory bus is to be connected[[,]];

enabling access, with a source and destination selector, to another memory bus, connected to one of the memory modules of the memory, from the incoming system bus or the memory access controller dependent on the first control signal/code received from the memory access controller[[,]]; and

selecting, with a memory module selector, which of the memory modules is to be connected to the outgoing system bus, connected to the memory accessing device, during a given read access of a specific one of the memory modules dependent on a second unique identifier.

23. – 25. (Canceled)